REMARKS

By this Amendment, it is proposed that the Drawings and Specification be amended to overcome the Examiner's objections. Claims 3 and 18 have been amended herein. Claims 1-22 remain pending in the application.

Section 112 rejection of Claims 3, 4, 10, 11, 15-17 and 20

Claims 3, 4, 10, 11, 15-17 and 20 were rejected under 35 USC 112, second paragraph. The Applicant respectfully traverses the rejection.

Claim 3

The Office Action rejected claim 3 for claiming "a second load" because it allegedly appears the current source switching circuit comprises two loads.

Claim 3 has been amended to overcome the rejection.

It is respectfully submitted that claim 3 is now in full conformance with 35 USC 2nd paragraph. It is therefore respectfully requested that the rejection be withdrawn.

Claim 10

The Examiner has rejected the recitation of "adapted to" as recited in claim 10 as allegedly being indefinite. The Applicant respectfully disagrees.

MPEP §2173.05(g) directs the Examiner to evaluate and consider a functional limitation for "what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used"(Emphasis added).

The limitation considered in *In re Hutchison* was "adapted to be adhered to a metal backing element for use in the fabrication of a template or the like", *Id.* at 140 (Emphasis added). The C.C.P.A has held that "...the introductory clause to the effect that the laminated article is "*adapted*" for use in making a template or the like ***does not constitute a limitation in any patentable sense..", *Id.* at 141 (italicizing original, underlining added).

As the MPEP §2173.05(g) correctly points out, the C.C.P.A. later

provided a **further clarification** on the issue of functional limitations in *In re Venezia*, 189 USPQ 149 (C.C.P.A. 1976). In considering a limitation, " a pair of sleeves....each sleeves of said pair adapted to be fitted over the insulating jacket of one of said cables.", *Id.* at 151, the court held:

> "Rather than a mere direction of activity to take place in the future, this language imparts a structural limitation to the sleeve. *** A similar situation exists with respect to the "adapted to be affixed" and "adapted to be positioned" *** "may be slideably positioned" *** "slideably positioned" *** this language also defines present structure or attributes **** a present structural configuration of the housing is defined in accordance with how the housing interrelates with the other structures in the completed assembly. We see nothing wrong in defining the structures of the components of the completed connector assembly in terms of the interrelationship of the components, or the attributes they must possess *** One skilled in the art would have no difficulty determining whether or not a particular collection of components infringe the collection of interrelated components defined by these claims.", Id. at 151-152 (Emphasis added).

The Applicant's recitations, "complementary pull-down mirror path transistor switch being adapted for operation opposite to that of said transistor switch" (claim 10) relates to the function of the pull-down mirror path transistor switch when powered. Of course, infringing devices may be sold in an unpowered state, and therefore would be 'adapted' to operate when powered by the purchaser.

Accordingly, it is respectfully requested that the rejection be withdrawn.

Claim 15

The Office Action alleges it is unclear how the current sink and current source relate to the load. Claim 15 is dependent on claim 2 which is dependent on claim 1. The claims must be read as a whole.

The claims clearly claim that the current source and current sink are connect to a first and second side of the claimed transistor. The transistor

switch and the pull down mirror path operate together to reduce charge injection flowing to a load. The current sink and current source are clearly claimed connected to the transistor switch. The transistor switch and the mirror path operate to reduce the charge injection flowing to a load. The structure of the claimed circuit is clear as claimed.

Claim 18

The Office Action rejected claim 18 as allegedly being indefinite under 35 USC 112.

The claims have been reviewed and are amended where appropriate. It is respectfully submitted that the claims are now in full conformance with 35 USC 112. It is respectfully requested that the rejection be withdrawn.

Claims 21 and 22

The Office Action alleges that the language "continuously receives said current flowing from said current source" is misleading from claims 21 and 22. The Applicant respectfully disagrees.

The Office Action alleges that the current from the current source flows to the load only when the transistor switch is conducting. The claims clearly claim the current is substantially continuously received by a load "when said transistor switch is opened". The claim must be read as a whole, not as individual steps taken out of context of the entire method. The claims are clear as written and support the language as the Office Action suggests is missing from the claims. The Applicant requests the rejection be withdrawn.

Claims not specifically addressed were rejected based on dependency. All the claims are in full conformance with 35 USC 112, and the Applicant requests the rejections be withdrawn.

Claims 1-5, 8-10 and 12-22 in view of Ravon

In the Office Action, claims 1-5, 8-10, 12 and 18-22 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by US Patent No. 6,137,275 to Ravon ("Ravon"), and claims 13-17 are rejected as obvious over Ravon. The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10 and 12-22 recite, *inter alia,* a transistor switch and a pull-down **mirror** path that operate to substantially continuously reduce charge injection flowing to a load.

Ravon appears to teach a system for providing a regulated voltage meant to supply a load (Ravon, Abstract). A current source providing the maximum current likely to be surged by the load, and a device for receiving the constant current and regulating the load supply voltage (Ravon, Abstract). A source 11 provides a constant voltage to a load, within a maximum current value that the load is likely to consume (Ravon, col. 3, lines 35-43). A regulating device 10 eliminates transients of the voltage supply to a load (Ravon, col. 3, lines 24-34). The regulating device includes a MOS power transistor M1, a MOS transistor M2, a transistor bias control circuit 13, and a comparator 14 (Ravon, Fig. 2; col. 3, line 49-col. 5, line 18). Transistor M2 controls the flow of current from the current source to ground (Ravon, Fig. 2). Transistor M1 controls the flow of current from the current source to the load (Ravon, Fig. 2).

Transistor M1 and M2 are not in a mirror paths (as alleged by the Office Action, page 7) for the current flowing from the current source to the load (Ravon, Fig. 2). The path through M1 flows current to the load, where the path through M2 flows the current to ground (Ravon, Fig. 2). Ravon fails to teach a transistor switch and a pull-down **mirror** path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 1-5, 8-10 and 12-22.

Ravon's system is designed to supply a regulated voltage, at varying currents but within a maximum surge current. Ravon's system is not concerned with charge injection, as Applicant's claimed invention. Charge invention is the current spike that occurs most frequently during a switch state of

either a MOS transistor switch or, more seriously, when a current source enters its saturation from a triod state, minority carriers from the inversion layer of the current source may be injected into the load. Ravon teaches the purpose of MOS transistor M2 is to absorb excess current during periods when the load only requires a low supply current. Excess current during periods when the load only requires a low supply current (col. 3, lines 59-62) is NOT charge injection, as claimed by claims 1-5, 8-10 and 12-22.

The Office Action alleges that although Ravon does not disclose the "substantially continuously" reduction of "charge injection" as recited in the claims, one of ordinary skill in the art would know it relates to the current required to charge the load capacitor (Office Action, page 7). The Examiner is mis-interpreting Applicant's claimed charge injection, since charge injection is NOT simply current required to charge a load capacitor. Charge injection is related to current spikes created during solid state switching. Ravon's disclosed circuit is not only different than the claimed invention, but is not even concerned with charge injection.

Accordingly, for at least all the above reasons, claims 1-5, 8-10 and 12-22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Ravon in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Ravon in view of Applicant's Admitted Prior Art Fig. 3 (AAPA). The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 of the present application recite, *inter alia,* a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

As discussed above, Ravon fails to teach a transistor switch and a pull-down **mirror** path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 1-5, 8-10 and 18-22.

The Office Action correctly acknowledged that Ravon fails to teach a serial combination of transistors. The Office Action relies on AAPA to make up for the deficiencies in Ravon to arrive at the claimed invention. The Applicant respectfully disagress.

AAPA teaches an unsatisfactory circuit for reducing charge injection which uses a serial combination of transistors forming a compensating switch (AAPA, Fig. 3). AAPA fails to teach a transistor switch and a pull-down **mirror** path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 6, 7 and 11.

AAPA and Ravon fail to teach a transistor switch and a pull-down **mirror** path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-5, 8-10 and 12-20 in view of Harston

In the Office Action, claims 1-5, 8-10 and 12-20 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over US Patent No. 5,343,196 to Harston ("Harston"). The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10 and 12-20 of the present application recite, *inter alia,* a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

Harston teaches a method of reducing the amount of current switched to a reference line so as to reduce the overall power consumption of a digital to analog converter (DAC). To achieve this, three transistors are employed. One MOS transistor acts as a current source. The two other

transistors act alternatively to direct current to **either** the load or **ground** (Harston, col. 1, line 41-42).

Harston fails to disclose a transistor switch and a **pull-down mirror path** operating to substantially continuously reduce charge injection flowing to a **load**. Harston's alternative parallel path flows current to **ground**, **NOT** to the capacitor 10pF and resistor at the OUTPUT. As seen in Harston's Fig. 3, the alternative path for the current coming from MP1 is to analog ground AGND, **NOT** to a load. There is **NO** mirror path since the alternate path goes to ground, **NOT** to OUTPUT (Harston, Fig. 3). MP3 is **NOT** a mirror path since the current does **NOT** flow to OUTPUT substantially **continuously**. If the current takes the MP3 path, **NO CURRENT** would flow to load OUTPUT (Harston, Fig. 3), since flowing to ground.

Accordingly, for at least all the above reasons, claims 1-5, 8-10 and 12-20 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Harston in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Harston in view of AAPA. The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 of the present application recite, *inter alia,* a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

As discussed above, Harston fails to teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 6, 7 and 11.

As discussed above, AAPA fails to teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 6, 7 and 11.

Harston and AAPA fails to teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Response to Arguments

Argument 1

The Office Action alleges that Applicant's recitation of charge injection in the preamble is not clearly distinguished from, or with the use of charge injection within the body of the claim. The Office Action states the charge injection related to the current source may not be the same as the charge injection flowing to the load, since the load could possibly be affected by charge injection from other circuitry (Office Action, page 14).

The opening paragraph of the argument section refers to claim 18, however the paragraph beginning with "1)" refers to claim 1, line 10. Since claim 1 does not have 10 lines, the Applicant is responding to claim 18.

The body of the claim now refers to "said charge injection", similarly recited in claim 1 which ties the preamble of the claim to the body of the claim, therefore referring to the same charge injection.

Argument 2

The Office Action alleges the current can not continuously be received by the load after opening the transistor when the only current path between the current source and load is open, as claimed by claims 21 and 22. The Office Action further alleges that the only way current IA from current source 420 can flow to load 440 is though switch 430, as shown in Fig. 5 (Office Action, page 15). The Applicant respectfully disagrees.

Claims 21 and 22 clearly claim opening a transistor switch connecting a current source to a load and, substantially simultaneously with the

step of opening, closing a switch to a pull-down mirror path in parallel with the transistor switch so that current from said current source flows through said pull-down mirror path. The claims clearly claim when the transistor is open, the switch in a pull-down mirror path is closed letting the current flow from the source to the load. Applicant's disclosure describing Fig. 5 at page 8, lines 2-7 support the claimed operation as claimed by claims 21 and 22.

Argument 3

The Office Action alleges Applicant clearly identified Harston's transistor MP3 as the pull-down mirror path which is in parallel to transistor switch MP2. The Office Action further alleges as long as transistor MP2 is off, and transistor MP3 is on, the charge injection (e.g. current) flowing to load 10pf is continuously reduced, in fact to zero (Office Action, page 15). The Applicant respectfully disagrees.

The Applicant never acknowledged Harston teaches a pull-down mirror path. Applicant is specifically arguing that Harston fails to teach a pull-down mirror path. The Examiner is completely misinterpreting the definition of a pull-down mirror path. Applicant discloses a pull-down mirror path in the disclosure as an alternate path for current to flow through to reach the load. The Examiner states Hartson's alternate path flows current to ground. As previously argued, ground is not a mirror path since the current destination is **NOT THE SAME** as the primary current path. The Examiner acknowledges the current destination in the alternate path is ground, so the Applicant is unclear as to how the Examiner maintains ground equates to a load. One branch directing current to ground and an alternate path directing current to a load (as disclosed by Harston) does NOT form a mirror path, as claimed.

The advantage of using a mirror path is that the current to the load is substantially continuous. Switching the current to ground creates a large period where the load is not supplied by a current, creating a large detriment to circuit speed delayed by a large period of current absence.

Argument 4

The Office Action alleges Applicant is relying on the claimed features, the mirror path current flowing to the load and continuous reduction of charge injection are not clearly recited in the rejected claims. The Office Action further alleges that Harston's transistors MP2 and MP3 can be considered mirror paths because one transistor is off while the other transistor is on. The Office Action further alleges that the claims do not recite when the "substantially continuously" reduction of charge injection actually occurs, and as long as Harston's transistor MP2 is off, and transistor MP3 is on, the charge injection (e.g. current) flowing to load is continuously reduced (Office Action, pages 15 and 16).

The continuous reduction of charge injection is clearly recited in the claims. It is unclear how having the terms within the claims and their interrelationship with other claim elements still leaves the terms un-clearly recited.

As discussed above, the Examiner is not reviewing the claimed limitation of a mirror path which is clearly claimed within the claims. The current path through Harston's transistors MP2 and MP3 are not mirrors. The current flowing through MP3 does not ultimately flow to the load. The current flowing through MP3 flows to ground as acknowledged by the Examiner.

As discussed above, charge injection is not simply current. Charge injection is a term of art having a very specific definition that the Examiner is taking as simply meaning current. The Examiner's argument clearly shows the Examiner is not considering the claimed limitations. If Applicant were concerned with simply reducing current to the load, the Applicant would have claimed a reduction of current to the load. Applicant is claiming a reduction of **charge injection**.

The charge injection is reduced whenever there is a need for the reduction. If there is never a need for charge injection reduction, then the mirror path would never operate to reduce the charge injection. When is dependent on need. The Applicant can not guess when there would be charge injection that

needs reduced. The Applicant simply claims the reduction of charge injection, meaning charge injection exists, and needs to be reduced. **When** would therefore be inherent within the claim equating to when charge injection exists.

Argument 5

The Office Action alleges one of ordinary skill in the art knows charge injection relates to charging currents, and even though Harston does not specifically disclose the reduction of charge injection, one of ordinary skill in the art can consider less current, or no current as one type of charge injection reduction (Office Action, page 16). Applicants respectfully disagree.

Charge injection is the undesired charge that may be injected from a switch transistor and/or a current source into a load which the current source is serving. As discussed above, the Examiner taking the definition of charge injection as simply current or relating to charging current , therefore, missing the limitations of the claims. Charge injection is a term of art, very specific beyond simply a reduction of current. The Examiner arguments, again, indicate the Examiner is not considering the claim limitations as recited. A term of art is to be read in the claims with its common definition. Any terms, not of art, can be defined by the Applicant. The Examiner is applying his own definitions to many of the claimed limitations, and ignoring definitions as defined within the art and Applicant's disclosure for others.

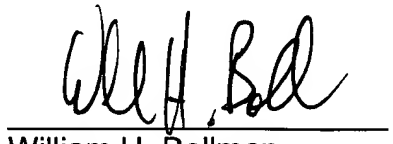
The claims are clear as written and the cited prior art not only fails to recited the claimed limitations, but also fails to disclose the claimed concepts. The Examiner is ignoring two of the most relevant limitations within the claims, a reduction of **charge injection** and a **mirror path**.

Conclusion

For at least all the above reasons, claims 1-22 are patentable over the prior art of record.

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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Version with Markings to Show Changes Made

3. (Twice Amended) The current source switching circuit according to claim 2, further comprising:

said first [a second] load connected between a ground and a second side of said transistor switch.

18. (Twice Amended) A method of reducing charge injection from a current source through a current switch into a load, said method comprising:

providing a pull-down mirror path in parallel with said current switch;

turning a switch in said pull-down mirror path on when said current switch is turned off; and

turning said switch in said pull-down mirror path off when said current switch is turned on;

wherein said current switch and said pull-down mirror path operate substantially continuously to reduce said charge injection flowing to said load.